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EXAMINER
ZAMAN, FAISAL M

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,312	SRINIVASAN ET AL.	
	Examiner	Art Unit	
	Faisal Zaman	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 4/11/2006 have been fully considered but they are not persuasive. Applicant argues that the newly added limitations to each of the independent claims are not taught in any of the references used in the original Office Action. However, these newly added limitations are in fact taught by Imperiali.

Applicant argues that the descriptor data in Imperiali (Column 4, lines 26-40 [e.g. data size information] and Column 6, lines 34-39 [e.g. address/location information]) does not teach including the location of the data to be operated upon and storing that descriptor data in the memory. However, this limitation is taught by Figure 4 of Imperiali, Column 6, lines 34-43, as the location of the data to be operated upon is stored in local address register 414. Imperiali does not expressly teach that the data size information is stored in a memory, but rather is sent to transfer size decoder block 232 for decoding. However, it would be obvious to one of ordinary skill in the art to use the data size information descriptor from the Interface 210 and combine it with the embodiment containing the location information descriptor of the DMA unit 410 (where both the data size information and the data location information would be stored in the local address register 414). The motivation to combine would be so in processing the data read request, the requesting device would be able to skip the step of determining the data size that needs to be retrieved from the system memory, since it is already contained with the local address information in the local address register 414.

Applicant also argues that Imperiali does not teach searching the memory (ie. in this case, the local address register 414) for the descriptor data associated with the read request. The DMA engine 412 searches the local address register 414 for an address corresponding to a read request from a device (Imperiali, Column 7, lines 7-15; ie. the DMA engine 412 requires the local address from the local address register 414 in order to complete the DMA request). With the combination of the data size information and data location information as described above, it would be obvious to one of ordinary skill in the art the data size information would also be searched along with the data location information.

Therefore, the rejection to Claims 1-28 as being unpatentable over the references used in the original Office Action stands, to the extent it has been claimed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1, 3-9, 11, 12, 14, 16, and 18-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bronson et al. ("Bronson") (U.S. Patent No. 6,973,528), in view of Imperiali (U.S. Patent No. 6,463,483).

Regarding Claims 1 and 16, Bronson discloses a device (Bronson, Figure 2, item 200, Column 3, lines 54-60) comprising:

A first port (Bronson, Figure 2, item 118, Column 3, lines 29-32) to allow the device to communicate with other devices (Bronson, Figure 2, item 126 and Figure 3, item 204, Column 3, lines 32-33 and lines 54-60) on an expansion bus (Bronson, Figure 3, item 206, Column 3, lines 58-62);

A second port (Bronson, Figure 2, item 124, Column 3, lines 29-30) to allow the device to communicate with devices (Bronson, Figure 2, items 112 and 114, and Figure 3, item 208, Column 3, lines 36-40 and lines 58-60) on a second bus (Bronson, Figure 3, item 210, Column 3, lines 60-62);

A memory to store data (Bronson, Figure 3, item 212, Column 4, lines 29-31); and

A processing element (Bronson, Figure 3, item 214 with 216, Column 3, lines 62-64) to:

Receive a read request from an expansion device (Bronson, Figure 3, item 250, Column 4, lines 14-16) to a predetermined area of system memory (Bronson, Figure 3, item 208, and Figure 2, item 114, Column 4, lines 14-28);

Transmit the read request to the system memory (Bronson, Figure 3, item 254, Column 4, lines 19-20);

Prefetch data from the system memory (Bronson, Column 4, lines 29-35).

Bronson does not expressly disclose the following limitations:

Receive descriptor data from the memory, wherein the descriptor data includes the location and size of the data to be operated upon;

Parse the descriptor data from the system memory to determine a data size.

Store the descriptor data in the memory; and

Search the memory for the descriptor data associated with the read request.

In the same field of endeavor (e.g. control of device buses in processor systems), Imperiali teaches:

Receiving descriptor data (Imperiali, Column 4, lines 13-20 and lines 36-42) from a memory, (Imperiali, Figure 2, items 12 and 14, Column 2, lines 64-66 and Column 3, lines 61-63) wherein the descriptor data includes the location (Imperiali, Column 6, lines 34-39) and size (Imperiali, Column 4, lines 26-40) of the data to be operated upon; and

Parsing the descriptor data from the system memory to determine a data size (Imperiali, Column 4, lines 36-42).

Store the descriptor data in the memory (Imperiali, Column 6, lines 34-43, ie. the location of the data to be operated upon is stored in local address register 414 and Imperiali, Column 4, lines 41-47; ie. it would be obvious to one of ordinary skill in the art to use the data size information descriptor from the Interface 210 and combine it with the embodiment containing the location information descriptor of the DMA unit 410 [where both the data size information and the data location information would be stored in the local address register 414]); and

Search the memory for the descriptor data associated with the read request (Imperiali, Column 7, lines 7-15; ie. the DMA engine 412 requires the local address from the local address register 414 in order to complete the DMA request and Imperiali, Column 4, lines 41-47; ie. with the combination of the data size information and data location information as described above, it would be obvious to one of ordinary skill in

the art the data size information would also be searched along with the data location information).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Imperiali's teachings of control of device buses in processor systems to the teachings of Bronson, for the purpose of increasing data throughput on the device bus (see Imperiali, Column 1, lines 26-27). Bronson also provides motivation to combine by stating it is an object of the invention to prevent data performance impacts when dealing with target devices that can only transfer data for a limited number of bytes before disconnecting (see Bronson, Column 2, lines 3-6).

Regarding Claim 3, Bronson teaches wherein the second bus further comprises a system bus (Bronson, Figure 2, Column 3, lines 24-29, ie. PCI bus 122 coupled to CPU 112 through Host bridge 120).

Regarding Claim 4, Bronson discloses wherein the second bus further comprises an expansion bus (Bronson, Column 3, lines 60-62, it is well known in the art that a PCI bus is a common type of expansion bus).

Regarding Claims 5-6 and 18-19, the examiner takes Official Notice that a device in the type of system disclosed is generally well-known in the art to comprise of a network device and/or an application specific integrated circuit, therefore it would be

obvious to one of ordinary skill in the art to use a network device and/or an application specific integrated circuit as the device in the claimed invention.

Regarding Claims 7 and 20, the examiner takes Official Notice that an expansion device in the type of system disclosed is generally well-known in the art to comprise of a network interface card, therefore it would be obvious to one of ordinary skill in the art to use a network interface card as the expansion device in the claimed invention.

Regarding Claim 8, all the same elements of Claim 1 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 1 applies equally as well to Claim 8.

Regarding Claim 9, all the same elements of Claim 2 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 2 applies equally as well to Claim 9.

Regarding Claim 11, Bronson discloses a method comprising disconnecting from the system memory once the data is received from the system memory (Bronson, Column 4, lines 38-46).

Regarding Claim 12, Bronson discloses a method comprising storing any prefetched data remaining for a read request if the expansion device disconnects (Bronson, Column 4, lines 56-64).

Regarding Claim 14, Bronson discloses a method comprising discarding any prefetched data not transmitted to expansion devices after a programmable amount of time (Bronson, Column 5, lines 8-17).

Claim Rejections - 35 USC § 103

4. **Claims 2, 10, 13, and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bronson in view of Imperiali as applied to Claim 1 above (hereinafter "Bronson-Imperiali"), in further view of Berry et al. ("Berry") (U.S. Patent No. 6,766,511).

Bronson-Imperiali discloses the invention substantially as claimed.

Bronson-Imperiali discloses the device of claim 1.

Regarding Claims 2 and 17, Bronson-Imperiali teaches a memory that comprises a storage (Imperiali, Figure 3, item 232 with item 232M and with item 224, Column 4, lines 13-15 and lines 36-40) in which to store packet addresses (Imperiali, Column 6, lines 34-43, ie. the location of the data to be operated upon is stored in local address register 414) and lengths (Imperiali, Column 4, lines 40-43, ie. "size of the data block") parsed from the descriptor data.

Bronson-Imperiali does not expressly disclose that the packet addresses and lengths are stored in a hash table.

In the same field of endeavor (e.g. storing data for executable modules), Berry teaches the use of a hash table for storing packet addresses and lengths (Berry, Column 26, lines 28-34).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Berry's teachings of storing data for executable modules with the teachings of Bronson-Imperiali, for the purpose of having efficient access to information (ie. descriptor data) related to a data packet. Bronson-Imperiali also provides motivation to combine by stating it is an object of the invention to increase data throughput on the device bus (see Imperiali, Column 1, lines 26-27).

Regarding Claim 10, Bronson-Imperiali teaches receiving a read request from the expansion device (Bronson, Column 4, lines 14-16);

Identifying the address for the read as not belonging to a preconfigured area of a system memory (Imperiali, Column 4, lines 13-18);

Accessing the data size from the descriptor data found in a storage (Imperiali, Column 4, lines 56-65 and Column 5, lines 43-55);

Issuing a read request to the system memory (Imperiali, Column 5, lines 1-55, the TX complete signal is the read request signal), wherein the read request has a request size based upon the data size (Imperiali, Column 5, lines 32-55, the data size is known); and

Transmitting data received in response to the read request to the system memory to the expansion device (Imperiali, Column 5, lines 17-21).

Bronson-Imperiali does not expressly disclose that the data size is stored in a hash table.

In the same field of endeavor, Berry teaches the use of a hash table for storing packet addresses and lengths (Berry, Column 26, lines 28-34).

The motivation used in the combination of Claim 2, super, applies equally as well to Claim 10.

Regarding Claim 13, Bronson-Imperiali teaches a method comprising accessing a storage within which are the descriptor data, including packet address and length (Imperiali, Column 4, lines 36-65).

Bronson-Imperiali does not expressly disclose that the packet addresses and lengths are stored in a hash table.

In the same field of endeavor, Berry teaches the use of a hash table for storing packet addresses and lengths (Berry, Column 26, lines 28-34).

The motivation used in the combination of Claim 2, super, applies equally as well to Claim 13.

Claim Rejections - 35 USC § 103

5. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Bronson-Imperiali as applied to Claim 1 above, in further view of Ong (U.S. Patent No. 5,815,662).

Bronson-Imperiali discloses the invention substantially as claimed.

Bronson-Imperiali discloses the method of claim 9.

Bronson-Imperiali does not expressly disclose the method further comprising:

Determining that the memory to store descriptors is full; and

Discarding an oldest descriptor entry.

In the same field of endeavor (e.g. scheduling of sending data across a network),

Ong discloses a method comprising:

Determining that the memory to store descriptors is full (Ong, Figure 2, item 30, Column 4, lines 22-24); and

Discarding an oldest descriptor entry (Ong, Figure 2, item 30, Column 4, lines 22-24).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Ong's teachings of scheduling of sending data across a network with the teachings of Bronson-Imperiali, for the purpose of minimizing unnecessary repetitive accesses to data storage devices (see Ong, Column 2, lines 23-27). Bronson-Imperiali also provides motivation to combine by stating it is an object of the invention to prevent data performance impacts when dealing with target devices that can only transfer data for a limited number of bytes before disconnecting (see Bronson, Column 2, lines 3-6).

Claims 21-28 are directed to an article of machine-readable code of the method of Claims 8-15. Bronson, Imperiali, Berry, and Ong teach, either alone or in combination as stated above, the method as set forth in Claims 8-15. Therefore,

Bronson, Imperiali, Berry, and Ong also teach, either alone or in combination as stated above, the article of machine-readable code as set forth in Claims 21-28.

Prior Art of Record

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Andrade et al. (U.S. Patent No. 5,649,161) discloses prepaging during PCI master initiated wait cycles. Shigeeda (U.S. Patent No. 5,737,765) discloses an electronic system with circuitry enabling access to configuration registers used by a memory controller. Gillespie et al. (U.S. Patent No. 5,913,045) discloses a programmable PCI interrupt routing mechanism. MacLaren (U.S. Patent No. 6,075,929) discloses prefetching data in response to a read transaction for which the requesting device relinquishes control of the data bus while awaiting data requested in the transaction. Batchelor et al. (U.S. Patent No. 6,286,074) discloses a method and system for reading prefetched data across a bridge system. Webber (U.S. Patent Publication No. 2003/0051076) discloses methods and a system for pre-fetching descriptors. Buckland et al. (U.S. Patent No. 6,665,753) discloses performance enhancement implementation through buffer management/bridge settings. Perez (U.S. Patent No. 6,820,161) discloses a mechanism for allowing PCI-PCI bridges to cache data without any coherency side effects. Easwar et al. (U.S. Patent No. 6,934,417) discloses determining if a memory is full and discarding an oldest entry in the case it is. Rosenberg ("Dictionary of Computers, Information Processing & Telecommunications")

discloses a definition (2) of hashing, which was used for the rejections in this Office Action.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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